

PowerDAQ CompactPCI/PXI Family

Simultaneous Sampling Multifunction Board



Features

- 4 single-ended simultaneous sample/hold A/D channels
- 300 kS/s–2 MS/s sampling rate
- 12-, 14-, 16-bit resolution
- Two 12-bit analog outputs; 32 digital I/O lines; three 16-bit counter/timers
- Simultaneous operation of all subsystems
- Stream-to-disk capability
- Calibration certificate included

PowerDAQ Software Suite

for Windows 9x/NT/2000/Me supports application development in Visual C++, Visual Basic, Delphi and C++ Builder.

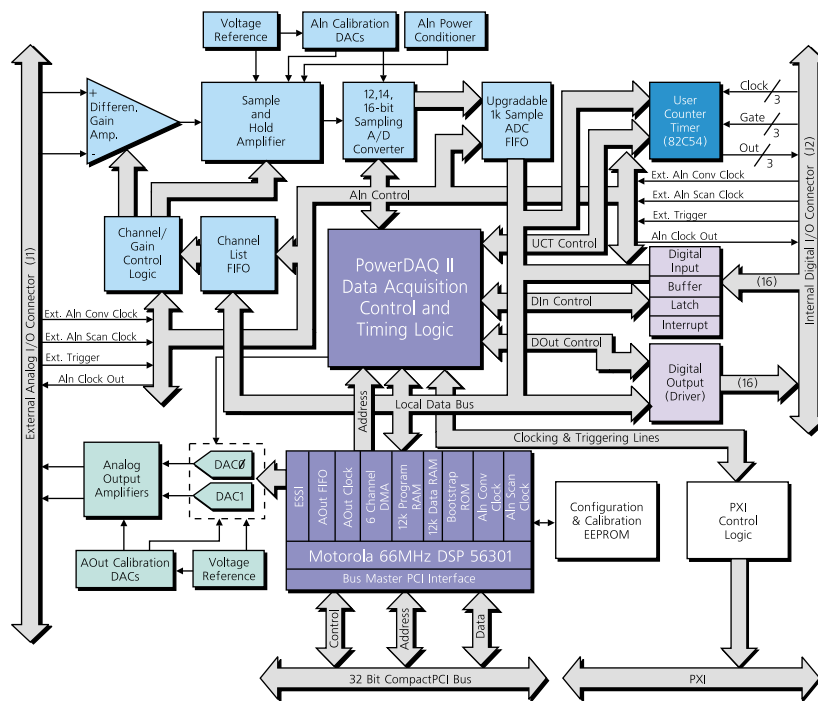
- PowerDAQ for Linux/RTLinux
- ProfessorDAQ Lite Excel Add-In
- PowerDAQ for QNX (optional purchase)

Also included at no cost are drivers for these applications: LabVIEW, Agilent VEE/VEE OneLAB, TestPoint, DASYLab, DIADem, MATLAB DAQ Toolbox

General Description

For some applications, it's essential to sample several channels at the same time within a few nanoseconds—a feat not possible with multiplexed multi-channel boards no matter how fast their burst rate across all the channels. For these tasks, UEI is proud to offer the PDXI-MFS Series, the only PCI boards currently available with as many as eight sample/hold amplifiers. This approach eliminates the need for expensive, bulky external simultaneous-sampling units. Not only do they offer the best in simultaneous sampling, they also come with the MF Series' array of other I/O capabilities including analog outputs, digital I/O and counter/timers.

PDXI-MFS boards build on all the power of the PDXI-MF Series including DSP control of all I/O subsystems. Here you have a choice of four or eight inputs running in either single-ended or differential modes. Three resolution grades and corresponding sampling rates are available: 16-bits (500 kS/s), 14 bits (500 kS/s, 800 kS/s and 2MS/s) or 12 bits (1 MS/s). In addition, you can purchase models with individual per-channel programmable-gain amplifiers.



PowerDAQ PDXI-MFS Block Diagram

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Technical Specifications

Analog Inputs

Model: PDXI-MFS-xx-	2M/14	1M/12	800/14	500/16	500/14	300/16
Resolution	14 bits	12 bits	14 bits	16 bits	14 bits	16 bits
Number of Channels						
Single-Ended	4 (8 optional)	4 (8 optional)	4 (8 optional)	4 (8 optional)	4 (8 optional)	4 (8 optional)
Differential	4 (8 optional)	4 (8 optional)	4 (8 optional)	4 (8 optional)	4 (8 optional)	4 (8 optional)
Maximum Sampling Rate (single or multiple channel)	2 MS/s	1.25 MS/s	800 kS/s	500 kS/s	500 kS/s	300 kS/s
Onboard FIFO Size (upgradeable to 16k, 32k, 64k)	4k samples	1k samples	1k samples	1k samples	1k samples	1k samples
Channel-Gain List	256 entries	256 entries	256 entries	256 entries	256 entries	256 entries
Input Ranges	0–5V, ±5V, 0–8V, ±8V @ 10V ranges	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)
Programmable Gains by channel	1, 2, 5, 10	1, 2, 5, 10	1, 2, 5, 10	1, 2, 5, 10	1, 2, 5, 10	1, 2, 5, 10
Drift						
Zero	±30 µV/°C	±30 µV/°C	±30 µV/°C	±30 µV/°C	±30 µV/°C	±30 µV/°C
Gain	±30 ppm/°C	±30 ppm/°C	±30 ppm/°C	±30 ppm/°C	±30 ppm/°C	±30 ppm/°C
Input Impedance	1 MΩ	1 MΩ	1 MΩ	1 MΩ	1 MΩ	1 MΩ
Input Bias Current	±100 pA	±100 pA	±100 pA	±100 pA	±100 pA	±100 pA
Input Overvoltage	±18V SE ±40V DI	±18V SE ±40V DI	±18V SE ±40V DI	±18V SE ±40V DI	±18V SE ±40V DI	±18V SE ±40V DI
A/D Conversion Time	0.45 µs	0.8 µs	1.25 µs	2 µs	2.0 µs	3 µs
SSH Amp Settling Time	0.7 µs	0.9 µs	1.0 µs	1.2 µs	1.2 µs	1.2 µs
A/D Settling Time	0.4 µs	0.6 µs	1.25 µs	1.5 µs	1.2 µs	2.7 µs
DC Accuracy						
Nonlinearity (no missing codes)	±2 LSB	±0.5 LSB	±0.5 LSB	±1 LSB	±1 LSB	±1 LSB
AC Accuracy						
Effective Number of Bits	12.1	11.3	12.7	13.8	12.7	13.8
Channel Crosstalk	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s
Clocking and Trigger Input						
Maximum A/D Pacer Clock Aggregate Throughput @ 0.01% accuracy	1600 kS/s @ 4 ch, 1800 kS/s @ 8 ch	975 kS/s @ 4 ch, 1095 kS/s @ 8 ch	800 kS/s	500 kS/s	500 kS/s	300 kS/s
External A/D Sample Clock Maximum Frequency	2 MHz	1.25 MHz	800 kHz	500 kHz	500 kHz	300 kHz
Minimum Pulse Width	20 ns	20 ns	20 ns	20 ns	20 ns	20 ns
External Digital (TTL) Trigger						
High-level Input Voltage	2.0V min	2.0V min	2.0V min	2.0V min	2.0V min	2.0V min
Low-level Input Voltage	0.8V min	0.8V min	0.8V min	0.8V min	0.8V min	0.8V min
Minimum Pulse Width	20 ns	20 ns	20 ns	20 ns	20 ns	20 ns

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Analog Outputs

	PDXI-MFS—all models
Number of Channels	2
Resolution	12 bits
Update Rate	200 kS/s each
Onboard FIFO Size	2k samples (on DSP)
Analog Output Range	±10V
Error	
Gain	±1 LSB
Zero	Calibrated to 0
Current Output	±20 mA max
Output Impedance	0.3Ω typ
Capacitive Drive Capability	1000 pF
Nonlinearity	±1 LSB
Protection	Short circuit to analog ground
Power-on Voltage	0V ±10 mV
Setting Time to 0.01% of FSR	10 μs, 20V step 1 μs, 100 mV step
Slew Rate	30 V/μs

Counter/Timer

	PDXI-MFS—all models
Number of Counters	3 available to user (Intel 82C54)
Resolution	16 bits on each counter
Clock Inputs	
Software configurable	Internal 1 MS/s, External ≤ 10 MS/s
High-level Input voltage	2.0V min
Low-level Input voltage	0.8V max
High-level Input current	20 μA
Low-level Input current	-20 μA
Gate Inputs	
Maximum Pulse Width	100 ns (high) 100 ns (low)
Counter Outputs	Inverted
Output Driver High Voltage	2.5V min (I _{OH} = 24 mA)
Output Driver Low Voltage	0.55V max (I _{OH} = 48 mA)

Digital I/O

	PDXI-MFS—all models
Input Bits (8 can generate IRQ)	16
Output Bits	16
Inputs	
High-level Input Voltage	2.0V min
Low-level Input Voltage	0.8V max
High-level Input Current	20 μA
Low-level Input Current	-20 μA
Outputs	
Output Driver High Voltage	2.5V min, 3.0V typ (I _{OH} = -32 mA)
Output Driver Low voltage:	0.55V max (I _{OL} = 64 mA)
Current Sink	-32/64 mA max, 250 mA per port
Pulse Width	20 ns min, interrupt bit latched on rising, falling or either edge
Power-on Voltage	Logic Zero

General Specifications and Connectors

	PDXI-MFS-All Models
Power Requirements	5V
Physical Dimensions	10.5" x 3.8" (262 mm x 98 mm)
Environmental	
Operating Temperature range	0°C to 70°C
Storage Temperature range	-25°C to 85°C
Relative Humidity	To 95%, noncondensing
Connector J1	96-pin high-density Fujitsu connector (male) (Fujitsu PN#FCN-245P096-G/U)
Connector J2	80-pin header connector (male) ???

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AGND	1	49	AGND
AGND	2	50	AQOUT0
AGND	3	51	AGND
AGND	4	52	AOUT1
DGND	5	53	AGND
AGND	6	54	AGND
AIN55	7	55	AIN54
AIN53	8	56	AIN52
AIN51	9	57	AIN50
AIN49	10	58	AIN48
AGND	11	59	AIN39
AIN38	12	60	AIN37
AIN36	13	61	AIN35
AIN34	14	62	AGND
AIN33	15	63	AIN32
AIN23	16	64	AIN22
AIN21	17	65	AIN20
AGND	18	66	AIN19
AIN18	19	67	AIN17
AIN16	20	68	AIN17
AIN6	21	69	AGND
AIN5	22	70	AIN4
AIN3	23	71	AIN2
AIN1	24	72	AIN0
AGND	25	73	AGND
DSP Trigger Input/AO External Clock	26	74	+5V (100 mA max)
ADC Conversion Start Out/ Pacer Clock Out	27	75	ADC Conversion Start Input / Pacer Clock
N/C	28	76	AGND
AGND	29	77	N/C
ADC Channel List Start Input / Burst Clock	30	78	AIN63
AIN62	31	79	AIN61
AIN60	32	80	AGND
AIN59	33	81	AIN58
AIN57	34	82	AIN56
AIN47	35	83	AIN46
AGND	36	84	AIN45
AIN44	37	85	AIN43
AIN42	38	86	AIN41
AIN40	39	87	AIN31
AGND	40	88	AIN30
AIN29	41	89	AIN28
AIN27	42	90	AIN26
AIN25	43	91	AGND
AIN24	44	92	AIN15
AIN14	45	93	AIN13
AIN12	46	94	AIN11
AGND	47	95	AIN10
AIN9	48	96	AIN8

DOUT11	1	2	DIN12
DIN13	3	4	DOUT10
DOUT12	5	6	DIN11
DIN14	7	8	DOUT9
DOUT13	9	10	DIN10
DIN15	11	12	DOUT8
DOUT14	13	14	DIN9
DOUT15	15	16	DGND
DGND	17	18	DIN8
DGND	19	20	+5VPI2
DGND	21	22	DGND
DGND	23	24	CL_DONE_OUT
DGND	25	26	CL_START_OUT_BACK
DGND	27	28	DGND
DGND	29	30	DGND
DGND	31	32	CL_START_OUT
DGND	33	34	CL_START_IN_BACK
DGND	35	36	DGND
DGND	37	38	TRIG_IN_BACK
DGND	39	40	DOUT7
DGND	41	42	CL_START_IN_BACK
DGND	43	44	DOUT6
DGND	45	46	DIN7
DGND	47	48	DOUT5
DGND	49	50	DIN6
DGND	51	52	DOUT4
DGND	53	54	DIN5
DGND	55	56	DOUT3
DGND	57	58	DIN4
DGND	59	60	DOUT2
DGND	61	62	DIN3
DGND	63	64	DOUT1
DGND	65	66	DIN2
UCT0_CLK_IN	67	68	DOUT0
UCT2_CLK_IN	69	70	DIN1
UCT0_OUT	71	72	DGND
UCT2_OUT	73	74	DIN0
UCT0_GATE	75	76	+5VPI2
UCT2_GATE	77	78	UCT_OUT
UCT1_CLK_IN	79	80	UCT_GATE

PowerDAQ II MFS Analog Connector (J1)

PowerDAQ II MFS Digital Connector (J2)

Ordering Information

PDXI-MFS-4-2M/142 MS/s, 14-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-8-2M/142 MS/s, 14-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-4-1M/121 MS/s, 12-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-8-1M/121 MS/s, 12-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-4-800/14800 kS/s, 14-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-8-800/14800 kS/s, 14-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-4-500/14500 kS/s, 14-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-8-500/14500 kS/s, 14-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-4-500/16500 kS/s, 16-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-8-500/16500 kS/s, 16-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-4-300/16300 kS/s, 16-bit, 4SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MFS-8-300/16300 kS/s, 16-bit, 8SE simultaneous sample & hold; two 12-bit D/As; 3 counter/timers; 32 digital I/O

Upgrade Options

PDXI-MFS-4-DG4Upgrade 4SE to 4DI with gains (1, 2, 5, 10)
PDXI-MFS-8-DG4Upgrade 8SE to 8DI with gains (1, 2, 5, 10)

Upgrade FIFO

PDXI-16KFIFOUpgrade 1K FIFO to 16K FIFO
PDXI-32KFIFOUpgrade 1K FIFO to 32K FIFO
PDXI-64KFIFOUpgrade 1K FIFO to 64K FIFO