PowerDAQ CompactPCI/PXI Family
A/D Multifunction Board

Features

- 16/64 single-ended or 8/32 differential A/D channels
- 150 kS/s–2.2 MS/s sampling rate
- 12-, 14-, 16-bit resolution
- Two 12-bit analog outputs; 32 digital I/O lines; three 16-bit counter/timers
- Simultaneous operation of all subsytems
- Stream-to-disk capability
- Calibration certificate included

PowerDAQ Software Suite
for Windows 9x/NT/2000/Me supports application development in Visual C++, Visual Basic, Delphi and C++ Builder.

- PowerDAQ for Linux/RTLinux
- ProfessorDAQ Lite Excel Add-In
- PowerDAQ for QNX (optional purchase)

Also included at no cost are drivers for these applications: LabVIEW, Agilent VEE/VEE OneLAB, TestPoint, DASYLab, DIADem, MATLAB DAQ Toolbox

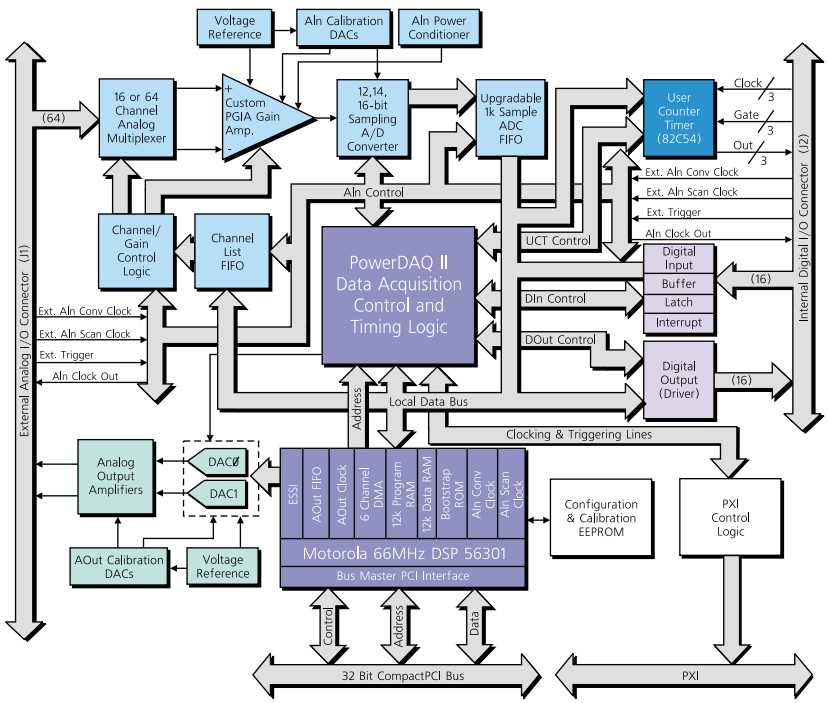
General Description

When you know you'll be setting up a stimulus/response test, a closed-loop system or if you just want to be ready for any kind of testing situation, a multifunction board is the logical choice. Our PDXI-MF Series boards pack everything you'll likely need: as many as 64 single-ended/32 differential analog inputs running at speeds to 2.2 MS/s, dual analog outputs, 32 digital I/O lines plus three counter/timers available to users.

To allow all these I/O subsystems to run simultaneously without loading down the host CPU, MF Series cards run under the control of a Motorola DSP. Thus you can collect analog samples while generating waveforms yet have the resources to perform digital I/O and run the counter/timers – all at the same time. Operating in this fashion presents no constraints on setup parameters, either: a custom PGIA (programmable-gain instrumentation amplifier) design runs any or all channels at different gains without the need to trade off peak throughput rate or accuracy.

We supply a complete set of drivers for all popular programming languages and third-party applications including LabVIEW and Agilent VEE – and at no additional charge! The support package also comes with example programs, complete with source code, that are so extensive that some of them might be enough to solve your problem straight out of the box.

To achieve optimum performance under Windows, we wrote the boards' 32-bit driver from scratch without relying on any legacy code. This advanced protocol-based driver works with shareable buffers in system RAM and makes obsolete traditional register-based drivers and double-buffering schemes. MF Series boards can stream data to disk continuously, gap-free, at the hardware's peak acquisition rates!



PowerDAQ PDXI-MF Block Diagram

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Technical Specifications

Analog Inputs

Model: PDXI-MF-xx-	2M/14H	1M/12x	500/16x	400/14x	333/16x	150/16x
Resolution	14 bits	12 bits	16 bits	14 bits	16 bits	16 bits
Number of Channels Single-Ended Differential	 16 or 64 8 or 32	 16 or 64 8 or 32	 16 or 64 8 or 32	 16 or 64 8 or 32	 16 or 64 8 or 32	 16 8
Maximum Sampling Rate (single or multiple channel)	2.2 MS/s	1.25 MS/s	500 kS/s	400 kS/s	333 kS/s	150 kS/s
Onboard FIFO Size (upgradeable to 16k, 32k, 64k)	4k samples	4k samples	2k samples	1k samples	1k samples	1k samples
Channel-Gain List	256 entries	256 entries	256 entries	256 entries	256 entries	256 entries
Input Ranges	0–5V, ±5V, 0–8V, ±8V @ 10V ranges	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)	0–5V, 0–10V ±5V, ±10V (software selectable)
Programmable Gains by channel	L=1,10,100,1000/ H=1, 2, 4, 8	L=1,10,100,1000/ H=1, 2, 4, 8	L=1,10,100,1000/ H=1, 2, 4, 8	L=1,10,100,1000/ H=1, 2, 4, 8	L=1,10,100,1000/ H=1, 2, 4, 8	L=1,10,100,1000/ H=1, 2, 4, 8
Drift Zero Gain	 ±30 µV/°C ±30 ppm/°C	 ±30 µV/°C ±30 ppm/°C	 ±30 µV/°C ±30 ppm/°C	 ±30 µV/°C ±30 ppm/°C	 ±30 µV/°C ±30 ppm/°C	 ±30 µV/°C ±30 ppm/°C
Input Impedance	10 MΩ	10 MΩ	10 MΩ	10 MΩ	10 MΩ	10 MΩ
Input Bias Current	±20 nA	±20 nA	±20 nA	±20 nA	±20 nA	±20 nA
Input Overvoltage	±20V,2000V ESD 10 mA max	±35V cont. 10 mA max	±35V cont. 10 mA max	±35V cont. 10 mA max	±35V cont. 10 mA max	±35V cont. 10 mA max
A/D Conversion Time	0.45 µs	0.8 µs	2 µs	2.5 µs	2.0 µs	20 µs
A/D Settling Time	0.37 µs	0.6 µs	1.2 µs	2.0 µs	1.2 µs	2.7 µs
DC Accuracy						
Nonlinearity	±2 LSB	±0.5 LSB	±1 LSB	±0.5 LSB	±1 LSB	±1 LSB
System Noise	1.2 LSB	0.3 LSB	1.3 LSB	0.8 LSB	1.3 LSB	1.2 LSB
AC Accuracy						
Effective Number of Bits	12.2	11.63	14.5	13.1	14.5	14.8
Total Harmonic Distortion+ Nonlinearity+Noise	76 dB	71.8 dB	88 dB	81 dB	89 dB	91 dB
Channel Crosstalk	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s	-80 dB @ 1 kS/s
Clocking and Trigger Input						
Maximum A/D Pacer Clock Aggregate Throughput @ 0.01% accuracy	 2200 kS/s @ 1 ch 1950 kS/s @ all	 1250 kS/s	 500 kS/s	 400 kS/s	 333 kS/s	 150 kS/s
External A/D Sample Clock Maximum Frequency	 2.2 MHz	 1.25 MHz	 500 kHz	 400 kHz	 333 kHz	 150 kHz
Minimum Pulse Width	20 ns	20 ns	20 ns	20 ns	20 ns	20 ns
External Digital (TTL)Trigger High-level Input Voltage Low-level Input Voltage Minimum Pulse Width	 2.0V min 0.8V min 20 ns	 2.0V min 0.8V min 20 ns	 2.0V min 0.8V min 20 ns	 2.0V min 0.8V min 20 ns	 2.0V min 0.8V min 20 ns	 2.0V min 0.8V min 20 ns

Analog Outputs

	PDXI-MF-all models
Number of Channels	2
Resolution	12 bits
Update Rate	200 kS/s each
Onboard FIFO Size	2k samples (on DSP)
Analog Output Range	±10V
Error	
Gain	±1 LSB
Zero	Calibrated to 0
Current Output	±20 mA max
Output Impedance	0.3Ω typ
Capacitive Drive Capability	1000 pF
Nonlinearity	±1 LSB
Protection	Short circuit to analog ground
Power-on Voltage	0V ±10 mV
Setting Time to 0.01% of FSR	10 µs, 20V step 1 µs, 100 mV step
Slew Rate	30 V/µs

Digital I/O

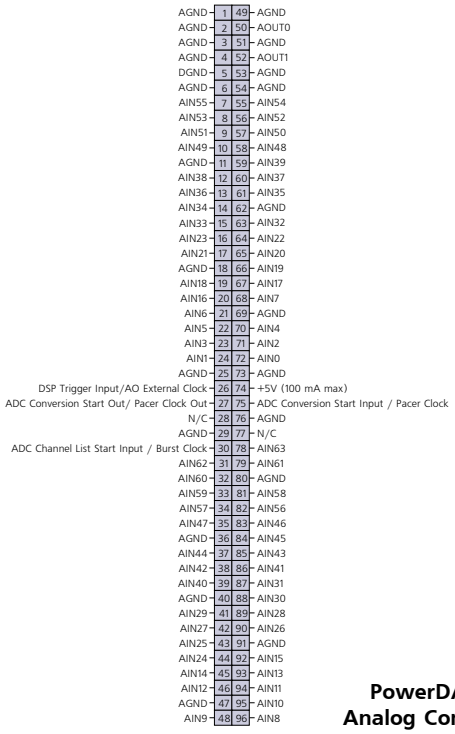
	PDXI-MF-all models
Input Bits (8 can generate IRQ)	16
Output Bits	16
Inputs	
High-level Input Voltage	2.0V min
Low-level Input Voltage	0.8V max
High-level Input Current	20 µA
Low-level Input Current	-20 µA
Outputs	
Output Driver High Voltage	2.5V min, 3.0V typ (I_{OH} = -32 mA)
Output Driver Low voltage:	0.55V max (I_{OL} = 64 mA)
Current Sink	-32/64 mA max, 250 mA per port
Pulse Width	20 ns min, interrupt bit latched on rising, falling or either edge
Power-on Voltage	Logic Zero

Counter/Timer

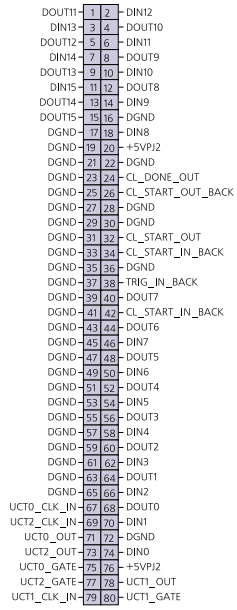
	PDXI-MF-all models
Number of Counters	3 available to user (Intel 82C54)
Resolution	16 bits on each counter
Clock Inputs	
Software configurable	Internal 1 MS/s, External ≤ 10 MS/s
High-level Input voltage	2.0V min
Low-level Input voltage	0.8V max
High-level Input current	20 µA
Low-level Input current	-20 µA
Gate Inputs	
Maximum Pulse Width	100 ns (high) 100 ns (low)
Counter Outputs	Inverted
Output Driver High Voltage	2.5V min (I_{OH} = 24 mA)
Output Driver Low Voltage	0.55V max (I_{OH} = 48 mA)

General Specifications and Connectors

	PDXI-MF-All Models
Power Requirements	5V
Physical Dimensions	10.5" x 3.8" (262 mm x 98 mm)
Environmental	
Operating Temperature range	0°C to 70°C
Storage Temperature range	-25°C to 85°C
Relative Humidity	To 95%, noncondensing
Connector J1	96-pin high-density Fujitsu connector (male) (Fujitsu PN#FCN-245P096-G/U)
Connector J2	80-pin header connector (male) ???



PowerDAQ II MF Analog Connector (J1)



PowerDAQ II MF Digital Connector (J2)

Ordering Information

PDXI-MF-16-2M/14H .....2.2 MS/s, 14-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-2M/14H .....2.2 MS/s, 14-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-1M/12L.....1.25 MS/s, 12-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-1M/12H.....1.25 MS/s, 12-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 Digital I/O
PDXI-MF-64-1M/12L .....1.25 MS/s, 12-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-1M/12H.....1.25 MS/s, 12-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-500/16L .....500 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-500/16H .....500 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-500/16L.....500 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-500/16H .....500 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-400/14L.....400 kS/s, 14-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-400/14H .....400 kS/s, 14-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-400/14L .....400 kS/s, 14-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-400/14H.....400 kS/s, 14-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-333/16L.....333 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-333/16H .....333 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-333/16L .....333 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-64-333/16H.....333 kS/s, 16-bit, 64SE/32DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-50/16L.....150 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,10,100,1000; two 12-bit D/As; 3 counter/timers; 32 digital I/O
PDXI-MF-16-50/16H .....150 kS/s, 16-bit, 16SE/8DI A/D, gains: 1,2,4,8; two 12-bit D/As; 3 counter/timers; 32 digital I/O

Upgrade FIFO

PDXI-16KFIFO .....Upgrade 1K FIFO to 16K FIFO
PDXI-32KFIFO .....Upgrade 1K FIFO to 32K FIFO
PDXI-64KFIFO .....Upgrade 1K FIFO to 64K FIFO